destination device IDs in a received frame) to the zone permission table. Specifically, the stored source zone group ID is applied to the zone permissions table as a first input and the destination zone group ID presently generated as the output of the CAM (memory circuit) is applied as a second input to the zone permissions table.

Processing of the two parallel threads discussed above is now converged to a single thread awaiting processing of the zone permissions table. Step **709** represents another pipeline stall to permit the zone permission table memory device to process its applied inputs (i.e., the two zone group IDs) and generate an output indicating whether or not the frame is permitted to be forwarded through the expander from the source device to the destination device. As above, step **709** represents any suitable number of clock cycles delay required for the zone permission table memory to process its applied inputs and generate its output permission signal. Step **710** then determines whether the zone permission table output indicates that the frame may be forwarded. If so, step **712** forwards the received frame on an appropriate port of the expander to the destination device. If not, step **714** returns an error indicator (e.g., a rejection) to the source device.

While the invention has been illustrated and described in the drawings and foregoing description, such illustration and description is to be considered as exemplary and not restrictive in character. One embodiment of the invention and minor variants thereof have been shown and described. In particular, features shown and described as exemplary software or firmware embodiments may be equivalently implemented as customized logic circuits and vice versa. Protection is desired for all changes and modifications that come within the spirit of the invention. Those skilled in the art will appreciate variations of the above-described embodiments that fall within the scope of the invention. As a result, the invention is not limited to the specific examples and illustrations discussed above, but only by the following claims and their equivalents.

What is claimed is:

1. A method for resolving source and destination information in a zoning SAS expander, the method comprising:
- receiving a frame, the frame including a source identifier identifying the source device and including a destination identifier identifying a destination device;
- resolving the source identifier to generate a source zone group identifier;
- resolving the destination identifier to generate a destination zone group identifier;
- applying the source zone group identifier and the destination zone group identifier to a zone permission table of the zoning SAS expander to determine if forwarding of the frame to the destination device is permitted based on the source zone group identifier and the destination zone group identifier; and
- forwarding the frame to the destination device responsive to a determination that forwarding of the frame is permitted.

2. The method of claim **1**
- wherein the step of resolving the source identifier further comprises applying the source identifier to a memory circuit to generate the source zone group identifier.

3. The method of claim **2**
- wherein the memory circuit is a content addressable memory circuit (CAM).

4. The method of claim **2**
- wherein the step of resolving the destination identifier further comprises applying the destination identifier to the memory circuit to generate the destination zone group identifier.

5. The method of claim **4** further comprising:
- delaying the step of applying the destination identifier to the memory circuit until the source identifier has been resolved by the memory circuit.

6. The method of claim **1** further comprising:
- storing the generated source zone group identifier prior to resolving the destination identifier to generate the destination zone group identifier,
- wherein the step of applying the source zone group identifier and destination zone group identifier further comprises:
- applying the saved source zone group identifier and the destination zone group identifier to the zone permission table.

7. Circuitry in a zoning SAS expander for full zone group identifier resolution in the zoning SAS expander, the circuitry comprising:
- a memory circuit adapted to store zone group identifier information for resolving a device identifier the memory circuit adapted to generate a device zone group identifier output in response to application of a device identifier input;
- control logic coupled with the memory circuit, the control logic adapted to apply a source identifier in a received SAS frame as an input to the memory circuit to generate a source zone group identifier and adapted to apply a destination identifier in the received SAS frame as an input to the memory circuit to generate a destination zone group identifier; and
- a zone permission table coupled with the control logic and coupled with the memory circuit, the zone permission table adapted to receive the source zone group identifier output and the destination zone group identifier output and adapted to determine if the received SAS frame may be forwarded to the device identified by the destination identifier based on the source zone group identifier and the destination zone group identifier,
- wherein the control logic is further adapted to forward the received SAS frame to the device identified by the destination identifier only if the zone permission determines that the received SAS frame may be forwarded to the device identified by the destination identifier.

8. The circuit of claim **7**
- wherein the memory circuit is a content addressable memory (CAM) circuit.

9. The circuit of claim **8**
- wherein the control logic further comprises:
- pipeline logic circuits configured to apply the source identifier to the CAM circuit during a first clock cycle of the multiple clock cycles and configured to apply the destination identifier to the CAM circuit during a subsequent clock cycle of the multiple clock cycles and configured to store the source zone group identifier generated by the CAM circuit as the destination zone group identifier is generated by the CAM circuit.

10. The circuit of claim **7**
- wherein the control logic further comprises:
- source identifier selection logic adapted to selectively override the source zone group identifier generated by the memory circuit and further adapted to generate the source zone group identifier based on information associated with the received SAS frame.

11. The circuit of claim **7**
- wherein the control logic further comprises:
- destination identifier selection logic adapted to selectively override the destination zone group identifier generated by the memory circuit and further adapted to generate